[0074] What is claimed is:

1. A method comprising:

applying logic operations to first and second differential pairs of periodic logic signals having a local frequency and to delayed versions thereof to produce a first differential pair of reference signals having relatively high spectral content at three times said local frequency and relatively low spectral content at other frequencies; and

mixing a differential pair of first input signals with said first differential pair of reference signals to produce a differential pair of first output signals having a dominant spectral component at three times said local frequency less a center frequency of said first input signals.

2. The method of claim 1, wherein applying said logic operations also produces a second differential pair of reference signals that is a delayed version of said first differential pair of reference signals, and said method further comprises:

mixing a differential pair of second input signals with said second differential pair of reference signals to produce a differential pair of second output signals having a dominant spectral component at three times said local frequency less a center frequency of said second input signals.

3. The method of claim 1,

wherein said first input signals are radio frequency signals and mixing said differential pair of first input signals with said first differential pair of reference signals includes down converting said input signals.

4. The method of claim 1,

wherein said first output signals are radio frequency signals and mixing said differential pair of first input signals with said first differential pair of reference signals includes up converting said input signals.

5. The method of claim 1,

wherein applying said logic operations includes applying said logic operations to produce said first differential pair of reference signals having a periodic pattern of three portions at a logic value interlaced with three portions at a different logic value.

6. The method of claim 1, further comprising:

generating said second differential pair of periodic logic signals with a phase delay of 90^{o} relative to said first differential pair of periodic logic signals;

generating a delayed version of said first differential pair of periodic logic signals with a phase delay of 45^{o} relative to said first differential pair of periodic logic signals; and

generating a delayed version of said second differential pair of periodic logic signals with a phase delay of 45^{o} relative to said second differential pair of periodic logic signals.

7. The method of claim 1, further comprising:

generating first and second differential pairs of substantially sinusoidal local oscillator signals; and

shaping said first and second differential pairs of local oscillator signals and delayed versions thereof to produce said first and second differential pairs of periodic logic signals and delayed versions thereof.

8. The method of claim 7, wherein generating said first and second differential pairs of substantially sinusoidal local oscillator signals includes generating said second differential pair of local oscillator signals with a phase delay of 90^{o} relative to said first differential pair of local oscillator signals, and said method further comprises:

generating a delayed version of said first differential pair of periodic local oscillator signals with a phase delay of 45^{o} relative to said first differential pair of periodic local oscillator signals; and

generating a delayed version of said second differential pair of periodic local oscillator signals with a phase delay of 45^{o} relative to said second differential pair of periodic local oscillator signals.

9. A method comprising:

mixing first and second differential pairs of local oscillator signals having a local frequency and a relatively low spectral content at three times said local frequency with a differential pair of input signals to produce a differential pair of output signals having a relatively high spectral content at three times said local frequency less a center frequency of said input signals.

10. The method of claim 9,

wherein said input signals are radio frequency signals and mixing said differential pair of input signals with said first and second differential pairs of local oscillator signals includes down converting said input signals.

11. The method of claim 9,

wherein said output signals are radio frequency signals and mixing said differential pair of input signals with said first and second differential pairs of local oscillator signals includes up converting said input signals.

12. The method of claim 9, further comprising:

generating said first and second differential pairs of local oscillator signals as substantially sinusoidal signals such that said second differential pair of local oscillator signals has a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 90^{o}.

13. The method of claim 12, wherein mixing said first differential pair of local oscillator signals with said differential pair of input signals further comprises:

generating a differential pair of mixer signals having half said phase difference relative to said first differential pair of local oscillator signals.

14. A method comprising:

mixing first, second and third differential pairs of local oscillator signals having a local frequency and relatively low spectral content at three times said local frequency with a differential pair of input signals to produce a differential pair of output signals having a relatively high spectral content at three times said local frequency less a center frequency of said input signals.

15. The method of claim 14,

wherein said input signals are radio frequency signals and mixing said differential pair of input signals with said first, second and third differential pairs of local oscillator signals includes down converting said input signals.

16. The method of claim 14,

wherein said output signals are radio frequency signals and mixing said differential pair of input signals with said first, second and third differential pairs of local oscillator signals includes up converting said input signals.

17. The method of claim 14, further comprising:

generating said first, second and third differential pairs of local oscillator signals as substantially sinusoidal signals such that said third differential pair of local oscillator signals has a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 120^{o}, and said second differential pair of local oscillator signals has half said phase difference relative to said first differential pair of local oscillator signals.

18. An integrated circuit comprising:

a logic circuit to apply logic operations to first and second differential pairs of periodic logic signals having a local frequency and to delayed versions thereof to produce a first differential pair of reference signals having relatively high spectral content at three times said local frequency and relatively low spectral content at other frequencies; and

a first mixer to mix a differential pair of first input signals with said first differential pair of reference signals to produce a differential pair of first output signals having a dominant spectral component at three times said local frequency less a center frequency of said first input signals.

19. The integrated circuit of claim 18, wherein said logic circuit is to produce a second differential pair of reference signals that is a delayed version of said first differential pair of reference signals, and the integrated circuit further comprises:

a second mixer to mix a differential pair of second input signals with said second differential pair of reference signals to produce a differential pair of second output signals having a dominant spectral component at three times said local frequency less a center frequency of said second input signals.

20. The integrated circuit of claim 18, further comprising:

a local oscillator to generate first and second differential pairs of substantially sinusoidal local oscillator signals; and

signal shapers to shape said first and second differential pairs of local oscillator signals and delayed versions thereof to produce said first and second differential pairs of periodic logic signals and delayed versions thereof.

21. An integrated circuit comprising:

a Gilbert cell active mixer having four branches and having three or more serially-connected transistors in each of said four branches.

22. The integrated circuit of claim 21, wherein said mixer further includes:

a first differential pair of input terminals to receive a first differential pair of local oscillator signals;

a second differential pair of input terminals to receive a second differential pair of local oscillator signals having a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 90^{o}; and

passive elements coupled to said transistors and to said first and second differential pairs of input terminals to generate a differential pair of mixer signals having a phase difference of substantially 45^{o} from both of said differential pairs of local oscillator signals.

23. The integrated circuit of claim 22, wherein said passive elements are resistive elements.

24. The integrated circuit of claim 22, wherein said passive elements are capacitive elements.

25. An integrated circuit comprising:

a quad-ring passive resistive mixer having four branches and having three or more serially-connected transistors in each of said four branches.

26. The integrated circuit of claim 25, wherein said transistors are field effect transistors.

27. The integrated circuit of claim 25, wherein said mixer further comprises:

a differential pair of input terminals;

a differential pair of output terminals;

a first node coupling a first and a second of said branches, and a second node coupling a third and a fourth of said branches, said first and second nodes connected to said differential pair of input terminals; and

a third node coupling said first and fourth branches, and a fourth node coupling said second and third branches, said third and fourth nodes connected to said differential pair of output terminals.

28. The integrated circuit of claim 25, wherein said mixer further comprises:

a first differential pair of reference input terminals to receive a first differential pair of local oscillator signals;

a second differential pair of reference input terminals to receive a second differential pair of local oscillator signals having a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 120^{o}; and

a third differential pair of reference input terminals to receive a third differential pair of local oscillator signals having half said phase difference relative to said first differential pair of local oscillator signals,

wherein gates of transistors in said first and third of said branches are connected to negative terminals of said reference input terminals, and gates of transistors in said second and fourth of said branches are connected to positive terminals of said reference input terminals.

29. A communication device comprising:

a monopole antenna; and

an integrated circuit coupled to said antenna, said integrated circuit including at least:

a logic circuit to apply logic operations to first and second differential pairs of periodic logic signals having a local frequency and to delayed versions thereof to produce a first differential pair of reference signals having relatively high spectral content at three times said local frequency and relatively low spectral content at other frequencies; and

a first mixer to mix a differential pair of first input signals with said first differential pair of reference signals to produce a differential pair of first output signals having a dominant spectral component at three times said local frequency less a center frequency of said first input signals.

30. The communication device of claim 29, wherein said logic circuit is to produce a second differential pair of reference signals that is a delayed version of said first differential pair of reference signals, and said integrated circuit further comprises:

a second mixer to mix a differential pair of second input signals with said second differential pair of reference signals to produce a differential pair of second output signals having a dominant spectral component at three times said local frequency less a center frequency of said second input signals.

31. The communication device of claim 29, wherein said integrated circuit further comprises:

a local oscillator to generate first and second differential pairs of substantially sinusoidal local oscillator signals; and

signal shapers to shape said first and second differential pairs of local oscillator signals and delayed versions thereof to produce said first and second differential pairs of periodic logic signals and delayed versions thereof.

32. A communication device comprising:

a monopole antenna; and

an integrated circuit coupled to said antenna, said integrated circuit including at least:

a Gilbert cell active mixer having four branches and having three or more serially-connected transistors in each of said four branches.

33. The communication device of claim 32, wherein said mixer further includes:

a first differential pair of input terminals to receive a first differential pair of local oscillator signals;

a second differential pair of input terminals to receive a second differential pair of local oscillator signals having a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 90^{o}; and

passive elements coupled to said transistors and to said first and second differential pairs of input terminals to generate a differential pair of mixer signals having a phase difference of substantially 45^{o} from both of said differential pairs of local oscillator signals.

34. The communication device of claim 33, wherein said passive elements are resistive elements.

35. The communication device of claim 33, wherein said passive elements are capacitive elements.

36. A communication device comprising:

a monopole antenna; and

an integrated circuit coupled to said antenna, said integrated circuit including at least:

a quad-ring passive resistive mixer having four branches and having three or more serially-connected transistors in each of said four branches.

37. The communication device of claim 36, wherein said transistors are field effect transistors.

38. The communication device of claim 36, wherein said mixer further comprises:

a differential pair of input terminals;

a differential pair of output terminals;

a first node coupling a first and a second of said branches, and a second node coupling a third and a fourth of said branches, said first and second nodes connected to said differential pair of input terminals; and

a third node coupling said first and fourth branches, and a fourth node coupling said second and third branches, said third and fourth nodes connected to said differential pair of output terminals.

39. The communication device of claim 36, wherein said mixer further comprises:

a first differential pair of reference input terminals to receive a first differential pair of local oscillator signals;

a second differential pair of reference input terminals to receive a second differential pair of local oscillator signals having a phase difference relative to said first differential pair of local oscillator signals, wherein an absolute value of said phase difference is substantially 120^{o}; and

a third differential pair of reference input terminals to receive a third differential pair of local oscillator signals having half said phase difference relative to said first differential pair of local oscillator signals,

wherein gates of transistors in said first and third of said branches are connected to negative terminals of said reference input terminals, and gates of transistors in said second and fourth of said branches are connected to positive terminals of said reference input terminals.